

ADVANCE PROGRAM

**2003 IEEE
BIPOLAR/BiCMOS
CIRCUITS AND
TECHNOLOGY MEETING**

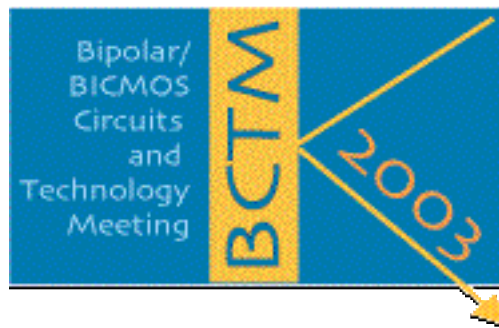
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**PIERRE BAUDIS CONVENTION CENTER
TOULOUSE, FRANCE**

SEPTEMBER 29 & 30, 2003

SHORT COURSE — SEPTEMBER 28, 2003

WORKSHOP on RF compact modeling — OCTOBER 1st



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**THE ELECTRON DEVICES SOCIETY OF
THE INSTITUTE OF ELECTRICAL AND
ELECTRONIC ENGINEERS**

IN COOPERATION WITH

THE IEEE SOLID-STATE CIRCUITS SOCIETY



2003 BCTM			
SCHEDULE AT A GLANCE			
Sunday — September 28			
8:00 AM — 5:15 PM	SHORT COURSE Cassiopée		
6:00 PM	Registration/Reception — Foyer Ariane		
Monday — September 29			
Registration open from 7:00 AM — Foyer Ariane			
8:00 AM	Opening Remarks and Announcements		
8:15 AM — 9:00AM	Keynote Speaker Prof. dr. Jan W. Slotboom The Shrinking Bipolar Transistor St. Exupéry Theatre		
9:00 AM	Vendor Exhibitions Open Coffee and Cookies — Foyer Ariane		
9:30 AM — 11:35 AM	1. Advanced Power Technology Ariane	2. Mixed-Signal Technology Options St. Exupéry	3. RF Circuit Blocks Cassiopée
11:35 AM — 1:20 PM	Lunch + Luncheon Speaker: Dr. Jean-Marie Chopin "Electronics for the Airbus world" Caravelle I		
1:30 PM — 3:10 PM	4. High-Speed Circuits St. Exupéry	5. Substrate Effects and Modeling Cassiopée	
3:10 PM	Coffee — Foyer Ariane		
3:30 PM — 5:35 PM	6. HBT Optimization Cassiopée	7. Thermal Parameter Extraction Cassiopée	
Author Interviews Immediately After Sessions			
7:00 PM 10:30 PM	Dinner Banquet Hôtel-Dieu St. Jacques		
Tuesday — September 30			
8:00 AM — 10:40 AM	9. Special Session: Emerging Technology/New Directions St. Exupéry Theatre		
10:40 AM	Coffee and Cookies — Foyer Ariane		
11:00 AM — 12:40 PM	10. Bipolar Device Physics Cassiopée	11. RF Transceivers St. Exupéry	
12:40 PM	Lunch/Exhibition Reception — Foyer Ariane		
2:30 PM — 4:35 PM	12. BiCMOS Platforms St. Exupéry	13. Noise and HF Characterization Cassiopée	
Author Interviews Immediately After Sessions			
Wednesday — October 1			
Workshop Compact Modeling For RF/Microwave Applications		Technical Tours AIRBUS CNES LAAS-CNRS MOTOROLA	

Welcome from the Chairmen

Welcome to the 2003 IEEE Bipolar/BiCMOS Circuits and Technology Meeting, the European premier of the BCTM in Toulouse, France. The growth in wireless communications and importance of SiGe HBTs for wireless products is reflected at BCTM this year in the large number of papers reporting advances in process technology and RF circuits.

The conference starts with a one day short course, followed by two full days of contributed and invited papers, including a special session on Emerging Technologies. The recent tradition of the BCTM Banquet continues on Monday evening. On Wednesday, there is workshop on Compact Device Modeling for RF/Microwave Applications organized by TU Delft, or the option to tours local technical facilities (Airbus Industrie, Motorola, LAAS and CNES). In addition, on Thursday there is a tour to Carcassonne, the largest walled city in Europe and one of the most perfectly preserved walled towns in the world. You can plan on spending a full five days enjoying the technical riches of BCTM, and savoring the history, beauty, and of course, the regional cuisine and wine in France's 4th largest city.

The short course features three renowned experts: Dr. Peter Magnée of Philips Research will lecture on SiGe device technologies, Prof. Hermann Schumacher of the University of Ulm will address MMIC design in SiGe processes, and Prof. Albert Wang on the Illinois Institute of Technology will cover ESD for RF and mixed-signal ICs.

We are fortunate indeed to have Prof.dr.ir. Jan Slotboom of TU Delft present the keynote speech, which will reflect on the advances in scaling of the bipolar transistor, based on his long and distinguished personal involvement.

The luncheon speech, by Dr. Jean-Marie Chopin of Airbus Industrie, will be on the development of the electronic "fly-by-wire" control of modern aircraft.

The technical program consists of 13 sessions with 42 contributed papers, 5 double-length invited papers, and 4 invited papers on Emerging Technologies. Prof. Jean Therme (LETI/CEA) reviews the nanotechnology scene in Europe, Dr. Joost van Beek (Philips Research) presents exciting developments in high quality passives for RF in silicon technologies, Dr. Jean-Luc Pelloie (SOISC) addresses SOI reliability issues, and Prof. Rashad Bashir (Purdue) describes fascinating work on the merging of microelectronics and microbiology.

We express our appreciation to the BCTM committee members for assembling a fine program for 2003, and to the local arrangements chair Marise Bafeur, for an outstanding job setting up the conference facilities and all of the local events. We hope you enjoy your visit to Toulouse and BCTM 2003.



Colin McAndrew
Conference General Chair



Ross Teggatz
Technical Program Chair

BCTM Short Course

High Speed SiGe HBT Device Design and Fabrication

Date: Sunday, September 28, 2003
Time: 8:00 AM - 5:15 PM
Location: **Cassiopée**

SiGe:C HBT Device Technology: What is the Big Deal?

Instructor: Dr. Peter Magnee, Philips Research, Leuven.

SiGe and SiGe:C heterojunction bipolar transistors (HBTs) are rapidly finding their way into radio-frequency (RF) BiCMOS technologies. Hence, a good understanding of the device behavior and fabrication process is of key importance. In this short-course, a brief tutorial is given on the device operation of Si/SiGe HBTs: why do we put SiGe in the base? Also, the effect(s) of incorporating of small amounts of C will be discussed.

SiGe and SiGe:C devices are fabricated by means of epitaxial growth. Different aspect of the various growth techniques will be reviewed, with the main focus on reduced-pressure chemical vapour deposition (RPCVD); selective growth versus non-selective growth, growth conditions versus C-incorporation, etc.

Finally, the way the HBT is integrated in a full, bipolar or BiCMOS, process has a significant impact on the device parasitics and hence, on the RF performance. An overview will be given on the different integration schemes that can be found in the literature, each with their own advantages and disadvantages.

Peter H.C. Magnee was born in Vlissingen, The Netherlands in 1969. He received his M.Sc. and Ph.D. degree in applied physics from the University of Groningen (The Netherlands) in 1991 and 1996 respectively. In 1996 he joined Philips Research in Eindhoven, where he worked in Si-based bipolar transistors for wide-band and RF-power applications.

In 2000 he moved, together with the Silicon Processing Technology Sector, to Philips Research Leuven. Since 2000 he is the project leader of the Advanced Bipolar/BiCMOS Technology project, which focuses on different technology- and device-options based on Si/SiGe heterojunction bipolar transistors. Dr. Magnee is a member of the Process Technology subcommittee of the BCTM.

Si/SiGe HBT MMIC design techniques for 20 GHz and beyond

Instructor: Professor Hermann Schumacher, University of Ulm

This course addresses the commercial relevance of silicon-based ICs and technologies for applications at 20 GHz and above. The requirements placed on SiGe HBT's for circuit design and operation at millimeter-wave frequencies is first examined. Passive devices and structures are critical to successful circuit implementations at these frequencies, and therefore the passive structures needed for micro and millimeter-wave IC implementations on a silicon substrate are discussed in detail. Important aspects of the design of monolithic microwave integrated circuits (MMIC's), including circuit topologies, physical layout, and substrate effects are then described. Circuits developed for operation at 24GHz and above will be used as design examples. Finally, a look ahead at how deep into the millimeter-wave range we may be able to reach in future is projected.

Hermann Schumacher was born in Siegen, Germany in 1957. He graduated with the Diplom-Ingenieur and Doktor-Ingenieur degrees from RWTH Aachen in 1982 and 1986, respectively. In 1986, he joined Bellcore (now Telcordia) in Red Bank, NJ as a Member of Technical Staff, working on InP-based planar photodetectors and heterojunction bipolar transistors.

In 1990, he became a professor at the University of Ulm, Germany. Since

then, his group has been working predominantly on Si/SiGe heterostructure devices and circuits, with special emphasis on receiver circuits and low-cost microwave ICs. He is the director of the Competence Center on Integrated Circuits in Communications at the University of Ulm (founded in 2001) and of the International Master Program on Communications Technology (established in 1998). Currently, he also serves as Vice President, Research, for the University of Ulm.

All About On-Chip ESD Protection Design: Mixed-Mode Simulation And ESD For RF/Mixed-Signal ICs

Instructor: Professor Albert Wang, Illinois Institute of Technology

ESD (Electro-Static Discharge) induced failure becomes a major IC reliability problem as IC technologies migrate into the VDSM ULSI regime. On-chip ESD protection circuitry is required to protect IC chips against ESD damages. Particularly, ESD protection design for mixed-signal & RF ICs emerges as a new challenge to IC designers. Unfortunately, trial-and-error approaches still dominate the current ESD design practices. This lecture intends to discuss all key aspects of practical ESD protection designs. It will cover the principles of ESD protection design, a new mixed-mode ESD simulation-design methodology developed at the Integrated Electronics Laboratory, Illinois Institute of Technology, and the unique problems for RF/mixed-signal ESD protection. Practical ESD protection circuit design examples will be provided. This lecture aims to assist IC designers in dealing with real-world ESD protection circuitry design problems.

Albert Wang received the BSEE degree from Tsinghua University, China, in 1985 and the Ph.D. in EE from the State University of New York at Buffalo in 1995. He was with National Semiconductor Corporation until 1998 when he joined the Faculty of Electrical and Computer Engineering of the Illinois Institute of Technology, where he is currently directing the Integrated Electronics Laboratory. His research interests center on analog/mixed-signal/RF ICs, advanced on-chip ESD protection, IC CAD and modeling, SoCs and semiconductor devices, etc. He received the CAREER Award from the National Science Foundation in 2002 and the Sigma Xi Award for Excellence in University Research from IIT in 2003. He is the author of the book *On-Chip ESD Protection for Integrated Circuits* (Kluwer, 2002, ISBN: 0-7923-7647-1), more than sixty papers in the field, and holds several U.S. patents. He is an Editor for the IEEE Electron Device Letters and an Associate Editor for the IEEE Transactions on Circuits and Systems II. He is an IEEE Distinguished Lecturer for the Electron Devices Society and the Solid-State Circuits Society, an IEEE EDS AdCom Member, Vice-Chair of EDS Regions and Chapters Committee for North America West and a Member of the EDS VLSI Technology and Circuits Committee. He serves as TPC Member, Sub-Committee Chair and Session Chair for many conferences, e.g., IEEE CICC, RFIC, APC-CAS, ASP-DAC, etc. He is an IEEE Senior Member, a frequent speaker at various industrial, academic, and international forums and a frequent consultant to the IC industry.

BCTM Short Course Schedule

High Speed SiGe HBT Device Design and Fabrication

Date: Sunday, September 28, 2002
Time: 8:00 AM - 5:15 PM
Location: **Cassiopée**

08:00-08:15 Welcome, Mikael Ostling, KTH Stockholm
08:15-09:15 SiGe:C HBT Device Technology: What is the Big Deal?
P.H.C. Magnee, Philips Research
09:15-09:40 Break
09:40-10:40 SiGe:C HBT Device Technology (continued)
10:40-11:00 Break
11:00-12:00 Si/SiGe HBT MMIC Design Techniques for 20 GHz and Beyond
H. Schumacher, University of Ulm
12:00-01:15 Lunch – **Caravelle 2**
01:15-02:15 Si/SiGe HBT MMIC Design Techniques (continued)
02:15-02:45 Break
02:45-03:45 All About On-Chip ESD Protection Design: Mixed-Mode Simulation and ESD for RF/Mixed-Signal ICs
A. Wang, Illinois Institute of Technology
03:45-04:00 Break
04:00-05:00 All About On-Chip ESD Protection Design (continued)
05:00-05:15 Course Evaluation

GENERAL INFORMATION

ADMISSION All interested persons are welcome to register and attend the BCTM. You do not have to be an IEEE member. Admission to sessions requires a BCTM badge. Please wear your badge at all times.

REFUNDS A full refund is available if you notify BCTM before the advance registration deadline that you cannot attend (Monday, September 8). Those who register but do not attend will receive a copy of the Proceedings (book & a CD-ROM) by mail after the meeting.

REGISTRATION On-line registration is the preferred method of registering this year. For further information see (www.ieee-bctm.org), the centerfold of this booklet, or contact:

Evelyne Trouvé	E-mail: bctm@laas.fr
LAAS/CNRS	Phone: +33-(0)56 133 6359
7 avenue du Colonel Roche	FAX: +33-(0)56 133 6208
31077 Toulouse, FRANCE	

LUNCHEON The BCTM luncheon is free to all registrants. It will be held on the opening day of the meeting, Monday, September 29.

DINNER BANQUET The dinner banquet will be held at the Hôtel-Dieu Saint-Jacques. This historic site was originally a stopover for pilgrims on the way to Santiago de Compostella. Founded in 1258, the complex of buildings is located on the right bank of the Garonne River, with an architectural style typical of the region. And the cuisine? Well, it's fantastically French, and you will be entertained by a Renaissance dance troupe. There is no charge to conference attendees. A limited number of tickets are available at 50.00 for additional guests on a first come, first serve basis.

OTHER CONFERENCE SOCIAL EVENTS Several events have been arranged to promote informal social interactions among conference participants. Sunday evening, from 6:00-9:00PM, the Foyer Ariane is open for registration with snacks and a cash bar. Following the Keynote speech and Emerging Technologies Sessions, coffee and cookies will be available and attendees will be able to meet new people and renew old acquaintances. Afternoon refreshment breaks provide another opportunity to interact. Tours of local technical facilities (Airbus Industrie, Motorola, LAAS and CNES) have been arranged for Wednesday, October 1 (the day after the conference).

TOURS A number of tours have been organized for spouses or partners who may be accompanying conference attendees. There is a: guided tour of Toulouse on Sunday morning (Sept. 28), a Garonne river cruise on Sunday afternoon, and a visit to the space center on Tuesday morning, Sept. 30. There is also a day-tour to the nearby historic walled town of Carcassonne on Thursday, October 2. Booking information is available via the website (www.ieee-bctm.org) under the "Program" menu.

SURROUNDING AREA Founded in the 4th century B.C., Toulouse is located in the heart of the Midi-Pyrénées region in the southwest of France. Its climate, the beauty of the natural surroundings, and the architectural environment provide ideal conditions for the lifestyle and activities that make this area so attractive. Toulouse is also the capital of the European aerospace industry, home of the second largest university campus in France with 110,000 students, and a major R&D center for advanced technologies.

TUTORIAL/SURVEY TALKS Tutorial talks given by invited experts are intended to give engineers who are not experts a broad overview of a given subject, and to offer a critical review of techniques and technology. They are twice the length of the usual contributed talk, and have longer abstracts in the Proceedings.

PROCEEDINGS A hard copy and a CD-ROM of the Proceedings are provided to each registrant. Additional copies can be obtained at prices shown in the registration centerfold in this booklet.

VENDOR EXHIBITS The BCTM Exhibits feature a host of well-established commercial vendors that support the bipolar/BiCMOS community. On Tuesday at 12:40PM, there is a hospitality luncheon in the *Foyer Ariane*. We invite you to join us for food/refreshment and to visit the vendor exhibits. All vendors must register if they wish to be present or post notices on the exhibits floor. Participating vendors will be allotted space in the *Foyer Ariane*. Contact Evelyne Trouvé LAAS/CNRS, 7 avenue du Colonel Roche 31077 Toulouse, FRANCE, e-mail: bctm@laas.fr, +33 (0)56 133 6359. The deadline for vendor space commitments is August 1, 2003.

MODELING WORKSHOP The one day workshop "Compact Device Modeling for RF/Microwave Applications" will be held on October 1 (after the conference) in Toulouse. Details are available on-line at (<http://ectm.et.tudelft.nl/cmrf03>).

AIRLINES & LOCAL TRANSPORTATION The closest airport is the Toulouse Blagnac Airport (www.toulouse.aerport.fr). The official carrier for BCTM 2003 is Air France, which offers excellent connections to Toulouse from most major centers. Information on discount fares with Air France is available at www.laas.fr/BCTM2003/AF_english.doc. A high-speed train service connects Toulouse and Paris via Bordeaux. Train timetables and fares are available at www.sncf.com. Discount fares for the train are also available. For more information see www.ieee-bctm.org.

HOTEL ACCOMODATIONS There are a number of excellent hotels within a short distance from the Pierre Baudis Convention Centre. For a list of hotels see the centerfold of this booklet or check our website (www.ieee-bctm.org) Please make your reservations early! When making reservations, be sure to inform the hotel that you are with "BCTM 2003" to receive the preferred conference rate.

MEMBERS OF THE PRESS The press is welcome to the BCTM and is offered FREE admission. Just present your business card at the registration desk. For advance information on the Meeting, call David Harame at (802) 769-9231 or send email to dharam@us.ibm.com.

FUTURE MEETINGS BCTM 2004 will be held at the Sheraton Centre, Montréal, Canada Sep. 12-14, 2004. David Harame, IBM Microelectronics, is Technical Program Committee Chair ((802) 769-9231, dharam@us.ibm.com). Local Arrangements Chair is Mourad El-Gamal (McGill U., (514) 398-7139, mourad@macs.ece.mcgill.ca). A description of the sites in Montréal can be found at: www.tourisme-montreal.org and www.montreal.com.

RECRUITING Intensive recruiting undermines the purposes for which the BCTM was established, and is contrary to IEEE policy. Those seen to be recruiting will be asked to surrender their badges and leave.

SUNDAY REGISTRATION AND SOCIAL HOUR 6:30-8:30PM Attendees can pick up badges and Proceedings on Sunday evening. Snacks and cash bar will be provided in the *Foyer Ariane*.

MONDAY EARLY REGISTRATION Registration will be open from 7:00 AM in the *Foyer Ariane*.

BEST STUDENT PAPER AWARD BCTM presents an award for the Outstanding Student Paper. To be considered for the award the student must be the lead author and speaker at the conference. The award consists of an engraved plaque and \$500.00, and is based on the technical quality of the published manuscript, clarity of the oral presentation, and the evaluation of the Technical Program Committee.

WELCOME AND OPENING REMARKS

8:00 - 8:15 AM — *St. Exupéry Theatre*

KEYNOTE SPEECH

8:15 - 9:00 AM — *St. Exupéry Theatre*

The Shrinking Bipolar Transistor

Jan W. Slotboom (Philips Research Fellow and Professor, Dept. of Electrical Engineering, Mathematics and Computer Science, Delft University of Technology)

After a short historical introduction, it will be shown that a number of new technologies has enabled the downscaling of the transistor dimensions. Most spectacular is the reduction of the base from about 30um to 0.03um.

Today we are in the middle of the breakthrough of the epitaxially grown SiGe(C) transistor. Simple device physics will be presented to explain how these new technologies can be exploited to push the transistor performance.

Some suggestions for future improvements, such as size reductions by 3D-integration and substrate transfer, steep and shallow junctions by laser annealing, as well as several new transistor structures with metal emitter or resurf collector, will be discussed.

9:00 – 9:30 AM – Vendor Exhibitions Open Break (Coffee and Cookies)

1. Advanced Power Technology

Monday AM — *Ariane*

Session Chair: Edouard de Fresart

Co-Chair: Joe Devore

(1.1) 9:30 – 9:55 AM – A Comparison of Bipolar Technologies for Linear Handset Power Amplifier Applications

Keith Nellis and Peter Zampardi (Skyworks Solutions Inc.)

This work evaluates four bipolar technologies that are currently competing to become, or remain as, the preferred bipolar technology for the commercial development of linear handset power amplifier modules. The four technologies are: GaAs HBT, Si BJT, SiGe HBT, and InP HBT. The purpose of this work is to evaluate each of these competing technologies in terms of linear handset PA requirements (i.e., P_{OUT} , ACPR, PAE, P_{GAIN} , and ruggedness).

(1.2) 9:55 – 10:20 AM — New Protection Structure Against Minority Carrier Injection

M. Zitouni, E. de Fresart, R. De Souza, X. Lin, J. Morrison, and P. Parris (Motorola SPS)

The purpose of this work is to find a solution to reduce the minority carrier injection impact on CMOS logic during inductive switching of a power device. This study was done by 2D and 3D device simulation.

(1.3) 10:20 – 10:45 AM — Non-Linear Electro-Thermal Model of an LDMOS Power Transistor Coupled to a 3D Thermal Model in a Circuit Simulator

Michael Guyonnet, Raymond Quéré, Raphael Sommet, Gérard Bouisse (Motorola, IRCOM)

In this article, we introduce a new approach to electro-thermal modeling of power LDMOS transistors. The electrical description of each intrinsic component is done with 3D bi-cubic splines. The electrical model is coupled to a 3D thermal model stemming from FEA simulation. This full 3D electro-thermal model is used with the ADS circuit simulator.

(1.4) 10:45 – 11:35 AM — Next Generation Semiconductors for DC-DC Converters (Invited)

Mohamed Darwish (Vishay-Siliconix)

The optimization of a new power trench MOSFET with W-shaped gate structure (WFET) for use in high efficiency synchronous buck DC-DC converters is investigated. A better trade-off between on-resistance and gate-drain capacitance is achieved using a thicker oxide at the bottom of the trench that is self-aligned to the P-body / N-epi junction. An optimized control switch with a low $R_{ds} \cdot Q_{gd}$ Figure of Merit of $10.5 \text{m}\Omega\text{-nC}$ is reported. Furthermore, an optimized synchronous switch is presented with a low gate-drain to gate-source charge ratio (Q_{gd}/Q_{gs}) of 0.45 for high shoot through immunity.

2. Mixed-Signal Technology Options

Tuesday AM — **St. Exupery**

Session Chair: Yih-Feng Chyan

Co-Chair: Angelo Pinto

(2.1) 9:30 – 10:20 AM — Cellular Radio Integration Strategies (Invited)

William Krenik and Jau-Yuann Yang (Texas Instruments)

The challenge to include color displays, games, audio, video, cameras, Bluetooth, WLAN, and multi-mode cellular in the same form-factor and power of today's handsets can only be met through aggressive integration of the handset electronics. This paper investigates one aspect of the integration challenge; the potential for integration of the handset radio functions with digital logic in advanced CMOS technology. Radio performance requirements, radio architectures, performance limitations of wafer process technology, development time, cost, and yield are investigated. Radio architectures suitable for integration are motivated and practical limitations are discussed.

(2.2) 10:20 – 10:45 AM — Copper Substrate Transfer Technology for Silicon RF Circuits

R. Dekker and C.E. Timmering (Philips Research)

We present exploratory experiments on the waferscale transfer of silicon RF circuits to copper substrates. This approach allows for a well defined microstrip transmission line interconnect and a perfect electrical and thermal grounding. Freestanding stress-free 6" transferred copper substrates are demonstrated and RF measurements on passive microstrip transmission lines are presented. Additionally, we present a new method enabling the dicing of these copper substrates. Perfect thermal and electrical grounding is advantageous for high performance RF power transistors for mobile communication and base stations.

(2.3) 10:45 – 11:10 AM — Dielectric Reliability and Material Properties of Al_2O_3 in Metal Insulator Metal capacitors (MIMCAP) for RF Bipolar technologies in comparison to SiO_2 , SiN and Ta_2O_5

K.-H. Allers, P. Brenner and M. Schrenk (Infineon)

We have characterized Al_2O_3 as a MIMCAP dielectric for RF bipolar technologies, including leakage current, reliability, C-V linearity and dielectric relaxation. These results are compared with more commonly known dielectrics: SiO_2 , SiN and Ta_2O_5 .

(2.4) 11:10 – 11:35 AM — A Comprehensive Experimental Study on Technology Options for Reduced Substrate Coupling in RF and High-Speed

Bipolar Circuits

M. Pfost, P. Brenner, T. Huttner, and A. Romanyuk (Infineon)

The influence of substrate coupling on advanced high-speed and RF circuits can have a significant impact on circuit performance and must therefore be reduced. Hence, the circuit designer usually applies shielding measures such as guard rings. In this work, different technology options such as high-resistivity and SOI substrates, transistor isolation techniques, and shielding methods are investigated, and their influence on substrate coupling is determined by measurements. The focus is on high-speed and RF circuits fabricated in advanced bipolar or BiCMOS technologies.

3. RF Circuit Blocks

Monday AM — **Cassiopée**

Session Chair: David Ngo

Co-Chair: Paul Davis

(3.1) 9:30 – 9:55 AM — A High Performance Unilateral 900 MHz LNA with Simultaneous Noise, Impedance, and IP3 Match

M.P. van der Heijden, L.C.N. de Vreede, F. van Straten, and J.N. Burghartz (TU Delft, Philips)

A 900 MHz LNA is presented, achieving 1.3dB NF, 15dB gain, -55dB isolation, and +10dBm IIP3 at 2.5mA, which is accomplished by an optimally designed out-of-band input termination and a current-feedback transformer with unilateralization capabilities.

(3.2) 9:55 – 10:20 AM — A 14.4mW, 1.6dB NF, 8.2GHz SiGe Bipolar LNA with DC Current Reuse

G. Gramegna, A. Magliarisi, M. Paparo (ST Microelectronics)

A balanced low-noise amplifier (LNA) is integrated in 0.25um BiCMOS with on-chip inductors. A DC current reuse scheme with Miller effect neutralization has been adopted in order to reduce power consumption and improve performance. At 8.2GHz the LNA features: 1.6dB NF, 21dB gain, output P-1dB of 3.3dBm, and drawing 14.4mW from a 1.8V supply. The LNA consumes an active area of 0.8x1.15mm².

(3.3) 10:20 – 10:45 AM — A BiCMOS SiGe Low Phase Noise Tunable 30 GHz RF Source Using a Frequency Tripler and a VCO

A. Coustou, D. Dubuc, J. Graffeuil, E. Tournier, O. Llopis, C. Boulanger, R. Plana and I. Telliez (LAAS-CNRS, STMicroelectronics, CNES, Université P. Sabatier)

A 10 to 30GHz tripler and X band VCO are integrated in a BiCMOS SiGe MMIC technology. These two circuits together implement a 30GHz source with -77dBc/Hz phase noise at a frequency offset of 100kHz.

(3.4) 10:45 – 11:10 AM — A 5GHz Low-Power Quadrature SiGe VCO with Automatic Amplitude Control

O. Mazouffre, .H. Lapuyade, .J.-B. Begueret, .A. Cathelin, D. Belot and Y. Deval (IXL, STMicroelectronics)

This paper presents a fully-integrated quadrature VCO and prescaler for HiperLAN2 applications. The circuit is implemented in a 0.25um SiGe BiCMOS process. The VCO and the prescaler are optimized for low voltage (<1.5V) and low power operation. The VCO draws 3mA and has an 18% frequency tuning range while exhibiting a phase noise of -93dBc/Hz at 1MHz offset from the 5.2GHz carrier. The measured amplitude and phase errors are less than 0.2dB and 3°. The integrated prescaler has a maximum frequency operation of 10GHz at a supply current of 1mA.

(3.5) 11:10-11:35 AM — A Fully Integrated 7-18GHz Power Amplifier with On-Chip Output Balun in

75GHz f_T SiGe Bipolar

W. Bakalski, A. Vasylyev, W. Simbürger, R. Thüringer, H.-D. Wohlmuth, A. Scholtz and P. Weger (Infineon, TU Vienna, TU Brandenburg)

An RF power amplifier for 7-18GHz operation with no external components was realized in a 75GHz- f_T , 0.35 μ m SiGe-BiCMOS technology. At 17.2GHz, the push-pull amplifier with integrated output balun delivers 12dBm at 1.2V and 17.5dBm at 2.4V.

Luncheon Monday

11:35 – 1:20 PM Caravelle I

Electronics for the Airbus world

Dr. Jean-Marie Chopin (Airbus Industrie, Toulouse, France)

Aviation has changed a lot during its one century history. Electronic technologies have to ensure at the same time:

- the largest performances and the more recent technologies,
- safety on applications and availability for a very long period of time.

Solutions are found all together with component technology selections, equipment design architectures and simulations.

4. High Speed Circuits

Monday PM – **St-Exupéry Theatre**

Session Chair: Mourad El-Gamal

Co-Chair: Dan Friedman

(4.1) 1:20 – 1:45 PM — A 98GHz Voltage-Controlled Oscillator in SiGe Bipolar Technology

W. Perndl, H. Knapp, K. Aufinger, T.F. Meister, W. Simbürger and A. Scholtz (TU Vienna, Infineon)

Two fully-integrated VCOs in a 200GHz f_T SiGe bipolar technology are presented. The oscillators use on-chip transmission lines for resonators and output impedance transformation. One oscillator operates up to 98GHz with a phase noise of -90.2dBc/Hz at 1MHz offset, can be tuned from 95.4 to 98.3GHz and consumes 12mA from a -5V supply. The second oscillator operates from 79.9GHz to 84.5GHz with a phase noise of -93.0dBc/Hz at 1MHz offset. These oscillation frequencies are the highest reported so far for fundamental mode oscillators in silicon-based technologies.

(4.2) 1:45 – 2:10 PM — A 24.9-GHz Emitter-Degenerated SiGe Bipolar VCO

J.H.C. Zhan, J.S. Duster, K.T. Kornegay (Cornell University)

A 24.9GHz emitter-degenerated VCO was fabricated in a 0.5 μ m SiGe BiCMOS process. It consumes 22mW from a 1.9V power supply including output buffers, exhibits -81dBc/Hz phase noise at 1MHz offset, and occupies 435x225 μ m².

(4.3) 2:10 – 2:35 PM — A 51GHz Master-Slave Latch and Static Frequency Divider in 0.18 μ m SiGe BiCMOS

A. Rylyakov (IBM)

A master-slave latch and companion 1:2, 1:4 and 1:8 static frequency dividers fabricated in 120GHz f_T SiGe operate at 51GHz, while drawing 30mA per latch (780mA total, with input-output buffers) from a -5.2V power supply.

(4.4) 2:35 – 3:00 PM — Static Bipolar 11GHz SiGe Divider with 1V Power Supply

S. Rylov and A. Rylyakov (IBM)

A low-voltage static 1:2 divider using CML gates with a single-transistor switching stack was designed in a 0.18 μ m SiGe BiCMOS technology. The

divider operates at 11GHz from a 1V supply and 16.2GHz from a 1.4V supply.

3:00 – 3:20 PM – Break (Coffee)

5. Substrate Effects and Modeling

Monday PM – **Cassiopée**

Session Chair: Jorg Berkner

Co-Chair: Jeroen Paasschens

(5.1) 1:20 – 2:10 PM — Substrate Modeling for RF and High-Speed Bipolar/BiCMOS Circuits (Invited Paper)

S. Strähle and M. Pfof (Infineon)

The undesired influence of the substrate on circuit performance cannot be neglected for many advanced high-speed and RF circuits and must therefore be modeled correctly already in the design phase. This paper gives an overview of the interaction between circuit components and the substrate, and reviews simulation techniques that can be used to determine its influence. In addition, the integration of substrate modeling into today's design environments will be discussed and explained by a practical example.

(5.2) 2:10 – 2:35 PM — An Accurate Method to Determine the Substrate Network Elements and Base Resistance

U. Basaran and M. Berroth (University of Stuttgart)

An accurate and robust method to determine the substrate network elements and base resistance of bipolar transistors from S-parameter measurements is proposed. The substrate network is compatible with large-signal models like HICUM and includes the substrate-collector depletion capacitance, substrate resistance and capacitance. The base resistance extraction method introduced in this work takes into account not only the extrinsic base-collector, but also the extrinsic base-emitter capacitance.

(5.3) 2:35 – 3:00 PM — Electrical Modeling of LSCRs in Deep Submicron CMOS Technologies for Circuit-Level Simulation of ESD Protection Structures

B. Caillard, F. Azaïs, P. Nouet, S. Dournelle and P. Salomé (LIRMM STMicroelectronics)

This paper presents an electrical model of a parasitic LSCR able to represent the inner currents before and after triggering. As an illustration, the model is used for the design of an advanced ESD protection structure.

3:00 – 3:20 PM – Break (Coffee)

6. HBT Optimization

Monday PM – **St-Exupéry Theatre**

Session Chair: Peter Magnee

Co-Chair: Alain Chantre

(6.1) 3:20 – 3:45 PM — SiGe Bipolar Technology with 3.9ps Gate Delay

T.F. Meister, H. Schäfer, K. Aufinger, R. Stengl, S. Boguth, R. Schreiter, M. Rest, H. Knapp, M. Wurzer, A. Mitchell, T. Böttner and J. Böck (Infineon)

A SiGe bipolar technology for future high frequency applications is presented. A cut-off frequency of 206GHz and a maximum oscillation

frequency of 197GHz combined with a state-of-the-art gate delay of 3.9ps has been obtained.

(6.2) 3:45 – 4:10 PM — Study On Extremely Thin Base SiGe:C HBTs Featuring Sub-5ps ECL Gate Delay

T. Tominari, S. Wada, K. Tokunaga, K. Koyu, M. Kubo, T. Udo, M. Seto, K. Ohhata, H. Hosoe, Y. Kiyota, K. Washio and T. Hashimoto (Hitachi)

A thin and heavily-boron-doped SiGe:C base was selectively grown by LPCVD. To achieve high-speed performance, we introduced carbon doping into the base region and studied As-grown intrinsic base width scaled-down towards 1nm with high process stability and high transistor yield. We realized f_T/f_{MAX} of 170/204GHz, ECL gate delay of 4.84ps, and a 57GHz maximum clock frequency of 16:1 MUX with this HBT.

(6.3) 4:10 – 4:35 PM — Vertical Profile Optimization of a Self-Aligned SiGeC HBT Process with an n-Cap Emitter

J.J.T.M. Donkers (Philips Research)

SiGeC HBTs with a cut-off frequency of $f_T > 150$ GHz have been realized with an n-type emitter cap, using a self-aligned integration scheme. Device simulations were used to tune the emitter base side of the non-selective epitaxially grown SiGeC layer. Experimental results are in very good agreement with the predictions.

(6.4) 4:35 - 5:00 PM — Integration of Selectively Implanted Collector (SIC) of SiGe:C HBT for Optimized Performance and Manufacturability

F.K. Chai (Motorola)

An investigation of various selectively implanted collector (SIC) integration options for SiGe:C HBT devices is reported. SIC integration before and after SiGe:C base epi as well as the size and concentration of the SIC region are evaluated. Tradeoffs between performance and manufacturability for various SIC integration options are discussed.

(6.5) 5:00 – 5:25 PM — A High Performance 0.18 μ m BiCMOS Technology Employing High Carbon Content in the Base Layer of the SiGe HBT to Achieve Low Variability of h_{FE}

S. Sawada (AnalogueLSI)

We present a 0.18 μ m BiCMOS technology in which h_{FE} variability of SiGe HBT is greatly minimized by means of increased neutral base recombination by adding high carbon content in the base layer. Device optimization yields peak f_T of 90GHz and peak f_{MAX} of 140GHz.

7. Thermal Parameter Extraction & ESD

Monday PM – **Cassiopée**

Session Chair: Guofu Niu

Co-Chair: Peter Zampardi

(7.1) 3:20 – 3:45 PM — Extraction and Modeling of Self-Heating and Mutual Thermal Coupling Impedance of Bipolar Transistors

N. Nenadovi_, S. Mijalkovi_, L.K. Nanver, L. K. Vandamme, H. Schellevis, V. d'Alessandro and J. W. Slotboom (TU Delft, TU Eindhoven, University of Naples)

Sensitive measurement of the self-heating and mutual thermal coupling impedance of bipolar transistors is performed with a low-distortion signal

generator and a lock-in amplifier. Thermal impedance is extracted and modeled for several silicon-on-glass test structures.

(7.2) 3:45 – 4:10 PM — Thermal Resistance of (H)BTs on Bulk Si, SOI and Glass

W.D. van Noort and R. Dekker (Philips Research)

Thermal resistance of SiGe HBTs and Si BJTs on bulk silicon, SOI, and glass is investigated. The analysis includes static, dynamic and mutual heating on glass. It is shown that a “floating” 10µm thick Cu island in close proximity to the device is already very effective to reduce the thermal resistance. A comprehensive method of thermal resistance extraction is presented.

(7.3) 4:10 – 4:35 PM — Solving ESD Protection Latchup Guard Rings Issue During Electrostatic Discharge (ESD) Events

D. Trémouilles, M. Bafleur, G. Bertrand, N. Nolhier, N. Mauran and L. Lescouzères (LAAS-CNRS, ON Semiconductor)

We show how latchup guard rings surrounding electrostatic discharges (ESD) protection devices, can reduce the overall performance of an ESD protection network. This issue is addressed by TCAD simulation and experimental results. Design guidelines to cope with this problem are proposed.

(7.4) 4:35 – 5:00 PM — Multi-Port ESD Protection Using Bi-Directional SCR Structures

V.A. Vashchenko, A. Concannon, M. ter Beek and P. Hopper (National Semiconductor)

A novel approach for the ESD protection of analog circuits using a pad-to-pad network is proposed and validated by numerical simulation and experimental data. The network is formed by inter-linked bi-directional SCR's. This network provides a space saving solution to the requirement for providing ESD protection for arbitrary pin-to-pin combinations and is especially attractive for small analog circuits in bipolar and BiCMOS technologies.

7:00 – 10:30 PM — Banquet (Hôtel-Dieu St. Jacques)

8. Emerging Technologies

Tuesday AM – *St. Exupéry Theatre*

Session Chair: Yih-Feng Chyan

(8.1) 8:00 – 8:40 AM — European Center for Innovations in Micro and Nano Technology (Invited)

Jean Therme (LETI/CEA)

In this presentation, we will describe programs and mechanisms for nanotechnologies in Europe, and describe some key results of European labs involved in this field. National initiatives aiming at setting-up European centers of excellence in the field of nanotechnologies are highlighted. We aim to show that the global profile of Europe in the field of nanotechnologies is rather low, but that this does not reflect the reality, as proven by recent results in the field of molecular electronics for instance. The European model for nanotechnologies development takes its strength in its multi-cultural and integrated approach to research and development.

(8.2) 8:40 – 9:20 AM — High-Q Integrated RF Passive and Micro-Mechanical Capacitors on Silicon (Invited)

Joost van Beek (Philips Research)

The PASSI™ technology platform is described for the integration of low-loss inductors, capacitors, and MEMS on high-ohmic Si substrates. Using this platform, the board space area taken up by e.g., impedance matching circuits can be reduced by 50%. The losses of passives induced by the semiconducting Si substrate can effectively be suppressed using a combination of surface amorphization and e-beam irradiation. The incorporation of MEM tuneable capacitors in high-Q inductor-capacitor networks is demonstrated.

(8.3) 9:20 – 10:00 AM — Reliability Issues in SOI Technologies and Circuits (Invited)

Jean-Luc Pelloie (SOISIC, France)

After explaining why SOI technologies bring higher speed, lower power consumption, higher integration and future CMOS perspectives, this paper addresses the reliability issues at the different stages of the development cycle: SOI wafer, device and circuit design.

(8.4) 10:00 – 10:40 AM — Interfacing Micro/Nano Technology with Life-Sciences for Detection of Cells and Micro-Organisms

R. Bashir, R. Gómez, H. Li, D. Akin and A. Gupta (Purdue University)

This paper reviews the interdisciplinary work performed in our group in recent years to develop micro-integrated devices to characterize biological entities. We present the use of electrical and mechanically based phenomena to perform characterization and various functions needed for integrated biochips. One system takes advantage of the dielectrophoretic effect to sort and concentrate cells within a micro-fluidic biochip. Another sub-system measures impedance changes produced by the metabolic activity of cells to determine their viability. A third device is used to detect the mass of bacteria as they bind to micro-mechanical silicon cantilevers. These devices with an electronic signal output can be very useful in producing practical systems for rapid detection and characterization of cells for a wide variety of applications in the food safety and health diagnostics industries.

10:40 – 11:00 AM — Break (Coffee and Cookies)

9. Bipolar Device Physics

Tuesday AM – *Cassiopée*

Session Chair: Marcel Tutt

Co-chair: Constantin Bulucea

(9.1) 11:00 – 11:50 AM — Improving IC Technologies Using Parametric Mismatch Characterization (Invited Paper)

H.P. Tuinhout (Philips Research)

This paper demonstrates that much better use of mismatch information is made if the process can be adapted based on mismatch fluctuation results early in the development cycle. This approach is based on the experience that parametric mismatch fluctuations and offsets provide insight into the microscopic architecture of integrated circuit devices. Several examples of how this insight can be used to improve the matching performance of BiCMOS technologies are given.

(9.2) 11:50 – 12:15 PM — Cryogenic Performance of a 200GHz SiGe HBT Technology

B. Banerjee, S. Venkataraman, Y. Lu, S. Nuttinck, D. Heo, Y.-J. Chen, J.D. Cressler, J. Laskar, G. Freeman, and D. Ahlgren (Georgia Tech, IBM)

The cryogenic performance of a 200GHz SiGe HBT technology is presented. At 85K, these SiGe HBTs maintain excellent *dc* ideality, with a peak current gain of 3800, a peak cut-off frequency of 26GHz, and a minimum noise figure of approximately 0.30dB at a frequency of 14GHz, and in all cases represent improvements over their corresponding 300K values. These results suggest that aggressively-scaled SiGe HBT technology is well-suited for emerging cryogenic applications requiring extreme levels of transistor performance.

(9.3) 12:15 – 12:40 PM — Impact of Collector-Base Junction Traps and High Injection Barrier Effect on 1/f Noise

J. Tang, G. Niu, A.J. Joseph and D.L. Hareme (Auburn U, IBM)

This paper investigates the impact of collector-base junction traps and high injection barrier effect on SiGe HBTs 1/f noise. CB junction traps result in higher I_B and higher base current 1/f noise at high injection.

10. RF Transceivers

Tuesday AM – **St-Exupéry Theater**

Session Chair: Leo de Vreede

Co-Chair: Sven Mattisson

(10.1) 11:00 – 11:25 AM — A Fully-Monolithic SiGe-BiCMOS Transceiver Chip for 24GHz Radar Applications

A. Ghazinour, P. Wennekers, J. Schmidt, Y. Yi, R. Reuter, J. Teplik (Motorola)

The design of a fully integrated 24GHz transceiver chip consisting of a differential VCO, a frequency divider and a mixer based on 0.35 μ m-BiCMOS technology is presented. Microstrip transmission lines are used as resonator and matching elements.

(10.2) 11:25 – 11:50 AM — A Precision Bipolar 5-6GHz Band Quadrature-Phase Generator

A. Chung, J.R. Long, P. van der Meer and D.L. Hareme (U Toronto, TU Delft, IBM)

A wideband bipolar doubler and high-sensitivity regenerative divider with precise I-Q phase tuning via a dc control are described. Measurements in the 5-6GHz band demonstrate that negligible residual phase noise is added by the circuit, which has an active area of just 0.26x0.11mm², consumes 23mW at 2.7V and has a phase tuning range of $\pm 22^\circ$ with 0.04 $^\circ$ /mV sensitivity.

(10.3) 11:50 - 12:40 PM — Frequency Synthesizers for RF Transceivers (Invited Paper)

D. Leenaerts and C. Vaucher (Philips Research)

Frequency synthesizers are used to generate the local oscillator (LO) signal in transceiver systems and act as the transceiver tuning system. In this presentation, an overview of commonly used state-of-the-art PLL architectures and its building block implementations will be discussed. Special attention will be paid to the design of the integrated LC-oscillator and the RF frequency dividers in advanced BiCMOS technologies. Some realized PLL designs for tuning systems will be presented. During the presentation, the relation between technology and design will be highlighted as well.

11. BiCMOS Platforms

Tuesday PM – **St-Exupéry Theater**

Session Chair: Vida Ilderem

Co-Chair: Alvin Joseph

(11.1) 2:30 – 2:55 PM — A Manufacturable 150GHz

f_T/f_{max} 0.13 μ m SiGe:C BiCMOS Technology

M. Laurens, B. Martinet, O. Kermarrec, Y. Campidelli, F. Deléglise, D. Dutartre, G. Troillard, D. Gloria, J. Bonnouvrier, R. Beerkens, V. Rousset, F. Leverd, A. Chantre and A. Monroy (STMicroelectronics)

This paper describes a manufacturable 0.13 μ m SiGe:C BiCMOS technology for optical networking and wireless applications, with npn f_T/f_{max} of 166/175GHz and 1.8V V_{CE0} , dual V_T and dual gate oxide CMOS devices, high quality passives and a 6-level copper back-end.

(11.2) 2:55 – 3:20 PM — A 0.13 μ m BiCMOS Technology Featuring a 200/280GHz (f_T/f_{max})SiGe HBT

B.A. Orner, Q.Z. Liu, B. Rainey, A. Stricker, P. Geiss, P. Gray, M. Zierak, M. Gordon, D. Collins, V. Ramachandran, W. Hodge, C. Willets, A. Joseph, J. Dunn, J.-S. Rieh, S.-J. Jeng, E. Eld, G. Freeman and D. Ahlgren (IBM)

We present for the first time a very high performance SiGe HBT with an f_T of 200GHz and f_{max} of 280GHz that has been successfully integrated with IBM's standard 0.13 μ m foundry-compatible CMOS node into our next generation BiCMOS technology.

(11.3) 3:20 – 3:45 PM — BiCMOS7RF: A Highly-Manufacturable 0.25- μ m BiCMOS RF-Applications-Dedicated Technology Using Non-Selective SiGe:C Epitaxy

H. Baudry, B. Szlag, F. Deléglise, M. Laurens, J. Mourier, F. Saguin, G. Troillard, A. Chantre and A. Monroy (STMicroelectronics)

This paper describes a new BiCMOS RF technology based on a mature 0.25 μ m CMOS process. Two SiGe:C HBTs are implemented for low and high voltage applications. Very low noise figure of 0.4dB at 2GHz is achieved. Other devices like isolated vertical PNP BJT, NLDEMOS and advanced passives are integrated in this technology to address RF circuit needs.

(11.4) 3:45 – 4:10 PM — A 5V Complementary-SiGe BiCMOS Technology for High-Speed Precision Analog Circuits

B. El-Kareh, S. Balster, W. Leitz, P. Steinmann, H. Yasuda, M. Corsi, K. Dawoodi, C. Dirnecker, P. Foglietti, A. Haeusler, P. Menz, M. Ramin, T. Scharnagl, M. Schiekofer, M. Schober, U. Schulz, L. Swanson, D. Tatman, M. Waitschull, J.W. Weijtmans and C. Willis (TI)

A novel complementary-SiGe BiCMOS technology developed for ultra-high speed precision analog circuits is presented. The modular process offers comparable NPN and PNP performance utilizing unique emitter interface and SiGe base processes.

(11.5) 4:10 – 4:35 PM — Vertical SiGe-Base Bipolar Transistors on CMOS-Compatible SOI Substrate

J. Cai, M. Kumar, M. Steigerwalt, H. Ho, K. Schonenberg, K. Stein, H. Chen, K. Jenkins, Q. Ouyang, P. Oldiges and Tak Ning (IBM)

We present a comprehensive experimental study of vertical SiGe-base bipolar transistors on 120nm SOI. Modulation of DC, RF and circuit performance by the SOI substrate bias is reported for the first time.

12. Noise and HF Characterization

Tuesday PM – **Cassiopée**

Session Chair: Didier Celi
Co-Chair : Thomas Zimmer

(12.1) 2:30 – 2:55 PM — Modeling the Correlation in the High-Frequency Noise of (Heterojunction) Bipolar Transistors using Charge-Partitioning

J.C.J. Paasschens, R.J. Havens and L.F. Tiemeijer (Philips Research)

We give a compact model formulation taking into account the correlation between the shot noise of the *intrinsic* base and collector current of bipolar transistors, based on the physical relation between noise and charge partitioning.

(12.2) 2:55 – 3:20 PM — An Examination of Bipolar Transistor Noise Modeling and Noise Physics Using Microscopic Noise Simulation

Y. Cui, G. Niu, and D.L. Harame 1 (Auburn U, IBM)

This paper examines bipolar transistor noise modeling and physics using microscopic noise simulation. Regional analysis is performed to identify the physical origins of model-simulation discrepancy.

(12.3) 3:20 – 3:45 PM — An Improved Method for Determining the Transit Time of Si/SiGe Bipolar Transistors

M. Malorny, M. Schröter, D. Celi and D. Berger (TU Dresden, STMicroelectronics)

An improved method for determining the transit time and forward-bias base-emitter depletion capacitance components from the transit frequency is presented. The method is verified and applied to experimental data of advanced Si/SiGe HBTs.

(12.4) 3:45 – 4:10 PM — Estimation of f_{\max} by the Common-Intercept Method

Z. Huszka, K. Molnár and E. Seebacher (Austriamicrosystems)

Recent technologies allow for such high device speeds that state of the art network analyzers can not directly measure the f_{\max} values. Extrapolation ratios exceeding a factor of three in terms of the upper frequency limit of the VNA are to be applied in some cases. A new constrained extrapolation method based on the common intercept of "passivity" curves is proposed to reduce the uncertainty in f_{\max} estimation.

Travel and Accommodation

For the most up to date information on travel and accommodation at BCTM 2003, visit www.ieee-bctm.org.

AIRLINES & LOCAL TRANSPORTATION The closest airport is the Toulouse Blagnac Airport (www.toulouse.aerport.fr). The official carrier for the BCTM 2003 conference is Air France, which offers excellent connections to Toulouse from most major centers. An attractive alternative is to use the SNCF high-speed train service connecting Toulouse (Matabiau station) and Paris via Bordeaux. Train timetables and fares are available online at www.sncf.com. Information on discounted fares (Air France and SNCF) is available from the BCTM website (www.ieee-bctm.org). Travel arrangements can be made through IEEE Global Travel Services. In North America call 800-879-4333 8:30AM-5:30PM EST Mon to Fri, or use their online travel service at www.ieee-travelonline.org. In many cases a rental car will not be necessary since the Meeting is located near the center of Toulouse and within easy walking distance of many sites, stores and restaurants. Public transit is also fast and efficient. To see sites outside of Toulouse a rental car is recommended. More information on tourism and travel to Toulouse and the Pierre Baudis Convention Center can be found at:
www.ot-toulouse.fr/English/venir/setvenir.html
www.centre-congres-toulouse.fr/english/english.html

HOTELS

The following is a short list of hotels close to Convention Center that are offering special prices (mention "BCTM 2003" when booking). A complete list of hotels in the Toulouse region is available online at www.ot-toulouse.fr/English/heberge/setheberge.html. Book early as space at these hotels is limited! At the time of writing, \$1 = €0.84.

Hotel Mercure ATRIA (before June 20)
Bvd Lascrosses, 8 esplanade Compans Caffarelli
Tel +33 5 61 11 09 09
FAX +33 5 61 23 14 12
SINGLE: €114.50, DOUBLE: €129, including continental breakfast

Hotel NOVOTEL Toulouse Centre (before July 28)
5 pl. Alfonse Jourdain
Tel +33 5 61 21 74 74
FAX +33 5 61 22 81 22
SINGLE: €107.50, DOUBLE: €118, including continental breakfast

Hotel de Brienne (before September 7 - just a few rooms)
20 Bvd Maréchal Leclerc
Tel +33 5 61 23 60 60
FAX +33 5 61 23 18 94
SINGLE/DOUBLE: €77 + €8.50 for continental breakfast

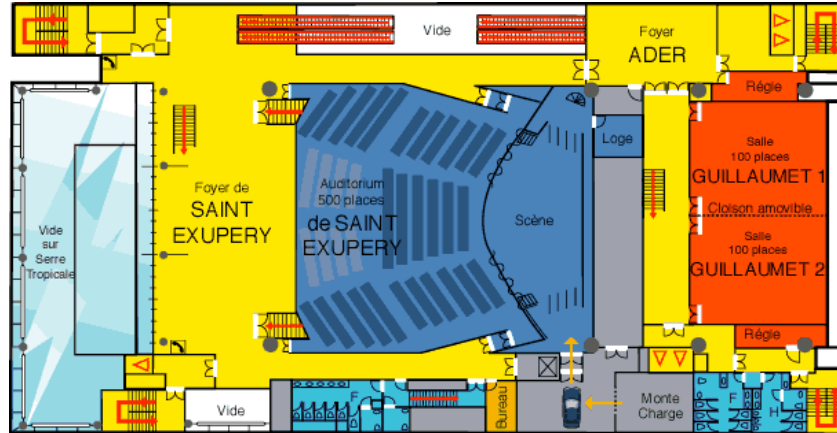
Hotel Crowne Plaza
7, place du Capitole
31000 Toulouse
Tel: +33 5 61 61 19 13 or +33 5 61 61 19 05
FAX: +33 5 61 23 79 96
e-mail: hicptoulouse@alliance-hospitality.com
SINGLE: €180 "Tradition" category room including continental breakfast (for 3 nights running) DOUBLE: €250 "Club Plaza" category room including continental breakfast (for 3 nights running)

Pierre Baudis Conference Center Floorplan

LEVEL 1



LEVEL 2



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