

NBTI-Resilient Memory Cells with NAND Gates for Highly-Ported Structures

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Abstract

NBTI is one of the most important sources of failure affecting transistors. NBTI degrades PMOS transistors whenever the voltage at the gate is negative (logic input “0”). Memory cells of storage blocks (e.g., register files) observe a “0” in the input of one of the two inverters at least 50% of the time.

This paper proposes a new memory-cell design for highly-ported structures consisting in a number of NAND gates arranged in a ring-manner that allows reducing the maximum degradation ratio due to NBTI below 50%.

1. Introduction

While technology evolution drives to smaller devices (transistors and wires), the supply voltage does not scale at the same pace, leading to higher current densities, which also produces higher temperatures. The increased current density and temperature accelerate transistor and wire degradation, and thus, shorten the lifetime of the product. Therefore, devices become more vulnerable from generation to generation. Moreover, the size of the chip does not scale, which implies that in every technology generation there is a larger number of such weak devices.

The increasing electric field and temperature make negative bias temperature instability (NBTI) [3][15] emerge as a threat for future technologies. NBTI affects basically PMOS transistors when negative voltage is applied at the gate (logic input “0”). Silicon-hydrogen bonds at the silicon/oxide interface break whenever a negative voltage is applied at the gate of the transistor, and hydrogen atoms are dragged away from the interface. The consequence is that some holes appear in the interface. Such holes trap some electrons when the transistor operates, and thus, the visible effect is an increase in the threshold voltage, and hence, a lower speed of the transistor.

Circuit degradation due to NBTI has an impact in the performance and power of circuits. The cycle time is impacted because circuits become slower when they degrade (if degradation is very high they may even stop working). The conventional solution to address the decrease of speed of circuits is guardbanding, which consists in decreasing the operating frequency by a given amount to account for the degradation that circuits may experience during their lifetime. Note that guardbanding is undesirable because significant performance is left on the table. Similarly, storage structures observe an increase of their V_{min} (minimum

voltage required to keep their contents) because of the NBTI aging [2][10]. Since V_{min} increases, the operating voltage cannot be decreased as much as desired for power savings.

Most of the area in the chips is devoted to memory-like structures such as caches, register files, etc. Bit cells of memory-like structures consist of a pair of inverters arranged in a ring-manner. The best case in terms of NBTI degradation happens when both PMOS transistors degrade the same (50% of the time each), because otherwise one of them degrades faster and fails earlier, meaning that the memory cell stops working.

Although data patterns are very biased for some bits, perfect balancing is achievable by timely inverting the contents of the cell [1][3]. Unfortunately, degradation ratios below 50% are unfeasible with conventional inverter-based memory cells.

This paper presents a new design for highly-ported memory cells consisting in a set of NAND gates arranged in such a way that the minimum degradation ratio for all PMOS transistors in the cell can be reduced; a design where N NANDS are employed achieves a degradation ratio of $1/N$. Such NAND-based memory cells show significant advantages for highly-ported structures such as register files with respect to conventional inverter-based cells. To the best of our knowledge this is the first attempt to mitigate NBTI in memory cells by reducing the maximum degradation of PMOS transistors below 50%.

By reducing the degradation due to NBTI the guardband of the different blocks can be reduced. Similarly, mitigating NBTI in memory-like structures provides energy savings due to a lower V_{min} .

The rest of the paper is organized as follows. Section 2 introduces the physics of NBTI. The NAND-cell design is presented in Section 3. Section 4 evaluates the NAND-cell design. Some related work is presented in Section 5. Finally, Section 6 draws the main conclusions of this work.

2. NBTI Source of Failure

NBTI has emerged as a significant issue for reliability of future technologies. This section illustrates the main mechanisms involved in NBTI degradation of transistors. First, we illustrate the physics behind NBTI. Then, we introduce the self-healing effect of NBTI that allows recovering from degradation. Finally, specific issues on NBTI in memory cells are described.

2.1 NBTI Physics

NBTI breaks progressively silicon-hydrogen bonds at the silicon/oxide interface whenever a negative voltage is applied

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to the gate of PMOS transistors [8][15]. Figure 1 illustrates the mechanisms of degradation. During degradation Si-H breakages generate more interface traps (N_{IT}), which capture electrons flowing from source to drain, leading to an increase of the threshold voltage (V_{TH}). Therefore, transistors become slower and may not fit the timing requirements, especially for those circuits that rely on a given relation between the delay of the pull-up and the pull-down. Whenever a transistor is under continuous degradation, its free hydrogen atoms are moved away from the interface.

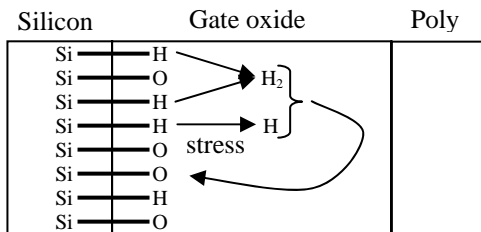


Figure 1. Physics of NBTI degradation and self-healing

Similarly to NBTI, PBTI (positive voltage temperature instability) affects NMOS transistors. While the physics of NBTI on PMOS transistors and PBTI on NMOS ones is basically the same, the degradation is significantly different. State-of-the-art experiments [9][13] have shown that PBTI degradation in NMOS transistors is negligible when compared to NBTI degradation in PMOS transistors.

Different parameters such as geometry, voltage, frequency, temperature and duty cycle (fraction of time with input set to “0” at the gate) of PMOS transistors have an effect on NBTI. They impact NBTI as follows:

- *Geometry.* While increasing the length of PMOS transistors increases the degradation due to NBTI [14][15], large width increase decreases such degradation [5] moderately.
- *Voltage.* The higher the operating voltage, the higher the degradation due to NBTI is [8][14].
- *Frequency.* Some studies show that NBTI is independent of the operating frequency [4], whereas other works show a weak dependence [1][3]: higher frequencies produce lower NBTI degradation. In any case the relation between frequency and NBTI degradation is low.
- *Temperature.* NBTI degradation is higher for higher operating temperatures [6][8][9].
- *Duty cycle.* Different studies have reported a strong dependence between the amount of NBTI degradation and the duty cycle [1][3]. The larger the amount of time with input set to “0”, the higher the degradation due to NBTI is.

2.2 NBTI Self-Healing Effect

A PMOS transistor degrades due to NBTI during those periods when its gate is set to “0”. Moreover, the higher the time the transistor observes a negative voltage at the gate, the farther the hydrogen atoms are dragged. Conversely, when its gate is set to “1” not only it does not degrade but it enjoys from the self-healing effect of NBTI [1][3][4][12]. During such periods, those hydrogen atoms that were dragged away

from the interface of the gate are dragged back to the interface filling the holes that they created (see Figure 1). The closer to the interface hydrogen atoms are, the faster they are dragged back to the interface. Hence, whenever the input at the gate of a PMOS transistor switches, hydrogen atoms are dragged back and forth to the interface providing a variable behavior of the transistor. NBTI degradation (self-healing effect) happens in such a way that the number of N_{IT} created (recovered) in the interface during a given period of time, Δt , is a fraction of the current number of Si-H bonds (H atoms). This behavior is illustrated in Figure 2, where periods of degradation and self-healing alternate¹. The straight line corresponds to simulation results whereas the dotted line shows measurements from real experiments. Note that V_{TH} shift depends directly on N_{IT} .

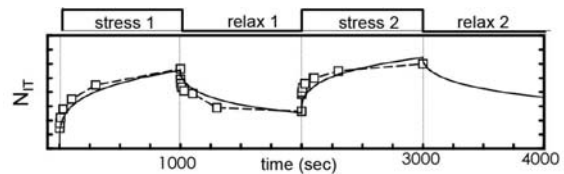


Figure 2. N_{IT} at the gate interface of a PMOS transistor during alternate periods of stress (gate set to “0”) and relax (gate set to “1”) [3]

As shown in the figure, degradation speed decreases as the number of Si-H bonds decreases (and hence, the N_{IT} increases). Recovery happens just the other way around: the higher the number of N_{IT} , the faster the recovery is. Full recovery could only happen after infinite relaxation time. As it can be seen, during relaxation periods degradation does not freeze but decreases, which implies that the benefits of keeping the gate of PMOS transistors set to “1” extends their lifetime significantly. NBTI is not well understood yet, so only chip testing can report real data on the lifetime increase (or guardband reduction) achieved by reducing the duty cycle of PMOS transistors. Nevertheless, some estimates [1][3] show that lifetime can be increased by a factor of at least 4X. Similarly, there is a lack of data reporting the benefits in terms of V_{min} that can be achieved if NBTI is mitigated although results are promising [2][10].

2.3 NBTI Issues in Memory Cells

Bit cells of memory-like structures consist of two inverters arranged in a ring-manner as shown in Figure 3. Hence, there is always one of the inverters with negative voltage (logic input “0”) in its gate, which implies that its PMOS transistor degrades. The best case degradation happens when the value at the output of each inverter is “0” 50% of the time, which means that both PMOS transistors degrade the same. Otherwise, one of such PMOS transistor degrades faster and the memory cell will fail earlier. Thus, it is desirable achieving a perfect balancing between the time that memory cells store “0” and “1”. Such perfect balancing can be achieved by different means. The easiest way consists in storing data inverted 50% of the time in such a way that what is biased to “0” in normal mode is biased to “1” in

¹ This picture has been taken from [3]

inverted mode, leading to an average bias of 50% in the long run [1][3][7]. Unfortunately, degradation ratios below 50% are unfeasible with inverted-based memory cells.

NBTI depends also on geometry of transistors as well as the operating voltage and frequency. Such parameters are set considering not only NBTI but power, area and delay of circuits, so changing them may have an impact in the whole processor design. Regarding temperature, it is not a parameter but an effect. Controlling the processor temperature has similar implications than the previously mentioned parameters. Thus, we focus only on the duty cycle.

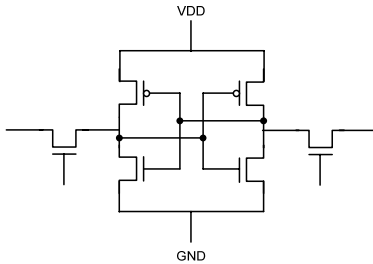


Figure 3. Design of a conventional bit cell

3. NAND-Based Memory Cells

In this paper we propose using NAND gates in bit cells instead of inverters to reduce the maximum degradation due to NBTI. The proposal consists in setting up a given number of NAND gates (N) with $N-1$ inputs each arranged in such a way that the output of each NAND gate is connected to the input of all the remaining NAND gates. This is illustrated in Figure 4 and Figure 5 for 3-NAND and 4-NAND cells respectively.

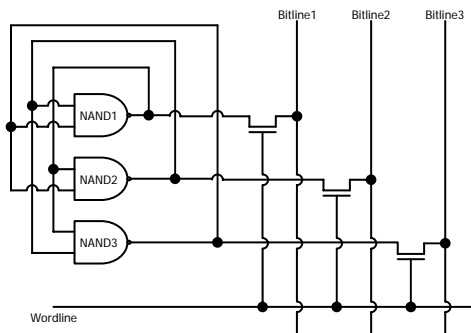


Figure 4. Single-ported 3-NAND cell design

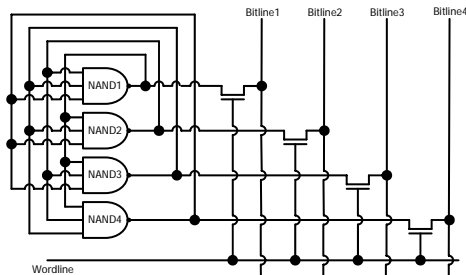


Figure 5. single-ported 4-NAND cell design

Due to the especial arrangement of the NAND gates, at any time there is one and only one NAND gate outputting a “0” whereas the rest of them output a “1”. The possible states for 3-NAND and 4-NAND cells are provided in Table 1 and Table 2 respectively. We can observe that NAND1 outputs a “0” in both cases, and thus, the rest of the NAND gates output “1”. In general, we have that all PMOS transistors attached to the NAND gate outputting a “0” observe a “0” in their gates ($N-1$ PMOS transistors) whereas the rest of transistors ($N-1$ PMOS transistors per NAND \times $N-1$ NAND gates) observe a “1” in their gate. Therefore, the ratio of PMOS transistors with a “0” in their gate (and hence, the degradation ratio) is $1/N$. For instance, the average degradation ratio of PMOS transistors is 33% (2 out of 6 PMOS transistors) for a 3-NAND cell, and 25% (3 out of 12 PMOS transistors) for a 4-NAND cell.

	Input1	Input2	Output
NAND1	1	1	0
NAND2	0	1	1
NAND3	0	1	1

Table 1. Example of inputs and outputs for a 3-NAND cell

	Input1	Input2	Input3	Output
NAND1	1	1	1	0
NAND2	0	1	1	1
NAND3	0	1	1	1
NAND4	0	1	1	1

Table 2. Example of inputs and outputs for a 4-NAND cell

It can be observed that the larger the number of NAND gates, the lower the average degradation is, but the higher the overhead of the new memory cell design. Another interesting observation is that the 2-NAND cell corresponds to the conventional memory cell with 2 inverters because we have 2 single input NAND gates (hence, inverters) with the output of each NAND gate connected to the input of the remaining NAND gates (hence, the other inverter). Thus, our proposal is a generalization of the conventional memory cells to mitigate the average degradation ratio due to NBTI.

Although the overhead in terms of area of NAND cells may be significant, it pays off due to two reasons:

- NAND cells have more states than conventional cells, and therefore, fewer cells are required to store the same amount of data. For instance, a 4-NAND cell has 4 different states (depending on which of the 4 NAND gates has the “0” on its output), and thus, a single cell can encode 2 bits.
- The number of bitlines required by a NAND cell grows linearly with the number of NAND gates, but if we consider the number of bits that it can store, we realize that the number of bitlines per bit of data remains constant. For instance, a 4-NAND cell stores 2 bits and has 4 bitlines (see Figure 5), which implies a cost of 2 bitlines per bit as in conventional inverter-based memory cells.

A first approximation to the cost of NAND cells is depicted in Table 3. We consider that each 4-NAND cell

encodes 2 bits. Similarly, each pair of 3-NAND cells encodes 3 bits because such pair of cells has 9 different states, which is enough to store 3 bits (8 different states). We can observe that the cost per bit only increases for the cell size, but not for the number of ports. Hence, the larger the number of ports, the lower the relative overhead of NAND cells is.

	Tx per cell	Tx per bit	BL per cell (each port)	BL and Tx per bit (each port)
2 inverters	4	4	2	2
3 NANDs	12	8 (3 bits in 2 cells)	3	2 (3 bits in 2 cells)
4 NANDs	24	12 (2 bits in 1 cell)	4	2 (2 bits in 1 cell)

Table 3. Transistors (Tx) and bitlines (BL) required for each type of memory cell

Two issues must be considered in the design of the new memory cells: the characteristics of the sense amplifiers and how data must be encoded/decoded to be stored in the NAND cells (this is important in order to achieve exactly the 1/N degradation in all PMOS transistors). These two issues are discussed in the following subsections.

3.1 Sense Amplifiers for NAND Cells

Conventional memory-like structures typically use differential sense amplifiers whose inputs are both the bitline and the inverted bitline of memory cells. Such type of sense amplifiers needs to be redesigned for NAND-based memory structures since, instead of sensing two lines (one of them outputting “0” and the other outputting “1”), sense amplifiers must read a larger number of lines (one of them outputting “0” and the rest of them outputting “1”).

An alternative to differential sense amplifiers consists in using single-ended sense amplifiers [16]. Such sense amplifiers require a single bitline as input. Note that they could be used for conventional memory structures too. In this case one of the sense amplifiers for each memory cell could be removed if needed, leaving one of the bitlines unread during read operation. The value from the unread bitline can be deduced from the other bitlines because both inverter-based and NAND-based memory cells output exactly one “0”, and thus, if no “0” is read means that the unread bitline outputs a “0”, otherwise it outputs a “1”.

3.2 Encoding and Decoding

To illustrate the logic required to encode/decode data for NAND-based memory cells we use the 4-NAND cells as a running example, and compare it with the inverter-based cells.

Encoding/decoding data for inverter-based memory cells is trivial. At write time, the identity bitline (BL1) is the written bit (B1) and the inverted bitline (BL2) just requires inverting B1. When reading, B1 can be obtained as the identity function of BL1. The 4-NAND cell needs a somewhat more complex mapping between the two input bits it can store (<B1, B2>) and the four bitlines (<BL1, BL2, BL3, BL4>). For instance, we can map data bits into bitlines as shown in Table 4.

B2	B1	BL4	BL3	BL2	BL1
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

Table 4. One possible mapping of input bits into bitlines for 4-NAND cells

To achieve the perfect balancing for the degradation of the PMOS transistors of memory cells, such cells must store each different value the same amount of time on average. In the case of inverter-based memory cells it can be easily achieved by having two different states that map B1 into BL1 and BL2 differently, and keeping the memory cells in each one of the two states 50% of the time. The two states can be encoded with a single bit (ST1). A possible mapping of B1 into BL1 and BL2 depending on ST1 is shown in Table 5. It can be seen that BL1 is computed as the XOR of ST1 and B1, whereas BL2 is computed as the XNOR of ST1 and B1.

The case for 4-NAND cells is a bit more complex because each cell can store 4 different values, and thus, we need 4 different states to map each value of the input (<B1, B2>) into each value of the bitlines (<BL1, BL2, BL3, BL4>) 25% of the time. Therefore, 2 bits for the state are required (ST1 and ST2). A possible mapping for the inputs into the bitlines is shown in Table 6. We can observe that the logic to encode/decode is quite simple. As an example we show the function to obtain BL4 when encoding (BL3, BL2 and BL1 functions are very similar) and the function to decode B2 (B1 function is very similar).

$$BL4 = (ST1 \oplus B1) + (ST2 \oplus B2)$$

$$B2 = \overline{ST2} \cdot \overline{BL2} + \overline{ST2} \cdot ST1 \cdot \overline{BL3} + ST2 \cdot \overline{ST1} \cdot \overline{BL3} + ST2 \cdot \overline{ST1} \cdot BL4 + \overline{ST2} \cdot \overline{ST1} \cdot BL4 \cdot BL3 + ST2 \cdot ST1 \cdot BL3 \cdot BL2$$

Table 5 and Table 6 provide mappings to encode/decode data so that the optimal balancing for the activity is achieved (all PMOS with “0” at their gate the same amount of time). In the running example it means that inverter-based cells observe degradation ratios of 50% in the PMOS transistors [7] whereas 4-NAND cells observe ratios of 25%. Hence, NAND-based cells show much lower degradation due to NBTI and their guardbands can be reduced and the performance boosted.

ST1	B1	BL2	BL1
0	0	1	0
0	1	0	1
1	0	0	1
1	1	1	0

Table 5. One possible mapping of input bits into bitlines for inverter-based cells with 2 different states

ST2	ST1	B2	B1	BL4	BL3	BL2	BL1
0	0	0	0	0	1	1	1
0	0	0	1	1	0	1	1
0	0	1	0	1	1	0	1
0	0	1	1	1	1	1	0
0	1	0	0	1	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	1	0	1	1
0	1	1	1	1	1	0	1
1	0	0	0	1	1	0	1
1	0	0	1	1	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	1	1
1	1	0	0	1	0	1	1
1	1	0	1	1	1	0	1
1	1	1	0	1	1	1	0
1	1	1	1	0	1	1	1

Table 6. One possible mapping of input bits into bitlines for NAND-based cells with 4 different states

4. Evaluation

This section provides a preliminary evaluation of the overhead of NAND-based memory structures with respect to conventional inverter-based ones in terms of delay, power and area. The evaluation has been done using CACTI [17], which is a timing, power and area model for cache-like structures.

Results are presented for a register file with 256 32-bit registers. The number of ports ranges between 1 and 16. The baseline is the inverter-based register file with perfect duty cycle. 3-NAND and 4-NAND cells register files are evaluated as well as two inverter-based baseline schemes all of them with perfect duty cycle:

- *Base x 2*. The whole register file is replicated in such a way that both register files can be used alternatively keeping one of them off at any time with the gated- V_{dd} mechanism [11]. In this way, degradation ratio of PMOS transistors reduces to 25% (50% during operation, and each register file operates 50% of the time). We consider that there is neither power nor delay overhead for this scheme. Such an optimistic assumption is against our proposal.
- *Base x 2 smart*. All bit cells are replicated but sharing the bitlines and wordlines. At any time only half of the bitcells work. The other half is turned off [11]. Each half can be used alternatively 50% of the time. Similarly to the *base x 2* scheme, the degradation ratio of PMOS transistors is 25%. A schematic of this approach is shown in Figure 6. This approach requires less area than the *base x 2* scheme. However, pass transistors for ports must be also replicated, which is still a significant overhead for highly-ported structures.

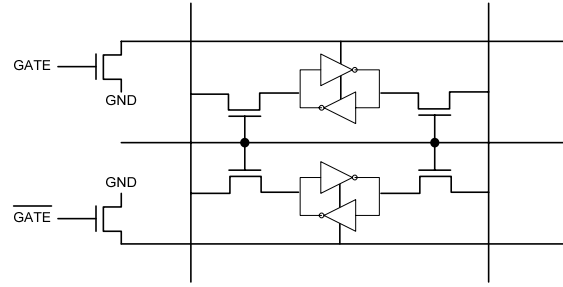


Figure 6. Schematic of a memory cell for *base x 2 smart* approach

Figure 7 (delay), Figure 8 (power) and Figure 9 (area) illustrate that using the 3- and 4-NAND cells has some overhead in terms of delay and area, but for large number of ports our designs pay off.

As we can see, the overhead in terms of delay for 3-NANDs cells is high due to the encode/decode complexity of such cells, but it is quite low for 4-NAND cells. For instance, for 9 ports the delay of the register file access is increased by 5% for 4-NAND cells. Furthermore, the benefits coming from the guardband shrinking are expected to be much more significant. The overhead in terms of power is negligible (below 1% in most of the cases). In terms of area, NAND-based cells are the best solution for highly-ported structures. For instance, the 4-NAND cells register file with 9 ports increases the area by 16%, which is much less than replicating the whole register file (*base x 2*) or replicating the memory cells (*base x 2 smart*).

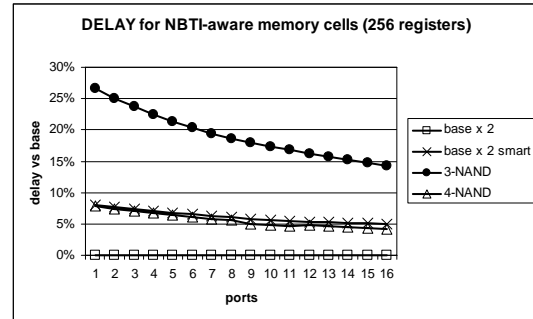


Figure 7. Delay for the different memory cells

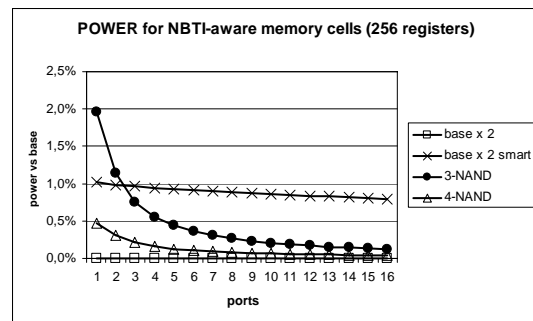


Figure 8. Power for the different memory cells

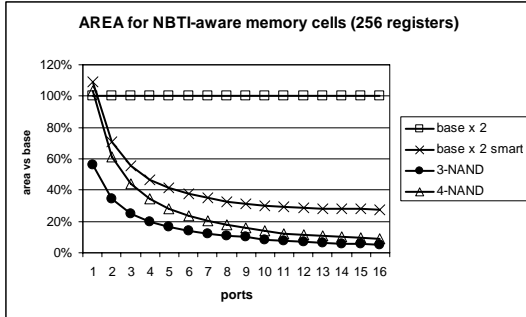


Figure 9. Area for the different memory cells

5. Related Work

Several works have focused on mitigating NBTI in PMOS transistors from the physics standpoint, and all of them are orthogonal with our approach. On the other hand, few attempts have been done to mitigate NBTI from the microarchitecture side. So far, only Xuan [18] has provided techniques to mitigate the impact of any source of failure by resizing the most vulnerable transistors of devices. Unfortunately, such a technique has a significant overhead for memory-like structures since all PMOS transistors in the cells of a memory structure have the same size and thus, all of them must be widened. As shown in the literature [5] PMOS transistors must be significantly widened to mitigate their degradation due to NBTI, making this solution too expensive for memory-like structures.

A mechanism to effectively achieve 50% duty cycle in conventional memory structures has been recently proposed [7]. Such mechanism is based on operating in inverted mode half of the time. To change from normal mode to inverted mode (or vice versa), data are read, inverted and written back, although simpler implementations may be used for structures where data can be evicted (e.g., caches).

To the best of our knowledge, the NAND-based memory cells proposed in this paper are the first approach to mitigate NBTI in PMOS transistors of highly-ported structures by decreasing the degradation ratio of transistors below 50%.

6. Conclusions

Current microprocessors leave significant performance and power on the road due to NBTI guardbands and increased V_{min} respectively. By reducing the amount of time that PMOS transistors observe a negative voltage at their gates NBTI is mitigated. However, memory cells cannot reduce that amount of time below 50%. In this paper we propose a new memory cell design for highly-ported structures that mitigates NBTI reducing the degradation of PMOS transistors down to 33%, 25% or even less. The new memory cell design is based on arranging NAND gates in such a way that only one of them outputs a "0" at any time.

Our results show that 4-NAND cells are a very suitable design for highly-ported memory structures like register files, providing much more reliable cells with low cost in delay, power and area. By mitigating the degradation due to NBTI, the guardband can be reduced leading to either higher performance or lower power dissipation, and the V_{min} can be decreased, which provides further energy savings.

Acknowledgements

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